# Layout Notes

For Reference Only

- 4-layer boards: interactive routing, stack-up in accordance with mechanical drawings (indicated with layer counts, requirements for layout and stack-up).

- Decoupling capacitor between all power supply ICs output and ground.
(note: unclear circuit drawings---often times engineers will skip this step)

- Ground power line width: 1.2~ 2.5mm; signal line width: 0.2~ 0.3mm; minimum spacing: 0.25mm (definition: line width, spacing).

- Power (ground) layer wiring: starting with power supply layer followed by the formation. It is best to retain the integrity of the formation (for EMC).

- (For mechanical restrictions) Please refer to the mechanical drawing for board frame, parts location, restrictions to part heights, and restrictions for layout(display of parts and traces are prohibited).

- (For automatic plug-in) The arrangement of parts should be done according to the SMT plug-in process. For example: the direction flow from the back side of SMD0603 and a tin oven forms a 90° angle. The DIP & IC components are on the front side.

- The parts must be organized and arranged in a good shape; the current of electrolytic capacitors for IC and DIP must go in the same direction.

- Component side has the tendency for vertical alignment; solder side has the tendency for horizontal alignment.

- Via size with drill = 12 pads = 24(mil).

- Avoid via holes within IC (QFP IC) except GND via.

- Distances between via and SMD pad should be 15mil and above.

- (For current stability) Additional 3~ 4 via holes near the output current and GND plane (front and back side & inside).

- (For Signal stability) No random signal lines are within BUS cable D0-D15 (A0 – A15).

- The Clock signal and USB signal (D+/D-) should be defined with the minimum trace lengths and being kept away from I/O Connector.

- (For EMC) Do not route clock and USB traces under crystals, oscillators and magnetic device.

- (For differential impedance) When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90°.

- (For differential impedance) Route all traces over continuous planes (VCC or GND) with no interruptions.

- (For differential impedance) Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 ohms differential impedance.

- (For differential impedance) USB designs require parallel termination at both the transmitter and receiver. The distances should be less than 200 mil (5.08mm).

- Position crystals and oscillators so that they lie flat against the PCB. Add a ground pad with the same or larger footprint under crystals and oscillators having multiple vias connecting to the ground plane.

- (Concern with appearance) Multi-gateway IC and exclusion can be reversed as needed (swap pin, swap gate).